#16

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Patent of

DAVID E. BOCCHI,
JEFFREY T. LAACKMAN and
STANLEY M. BACH, JR.

For

IMPLANTABLE N-PHASIC DEFIBRILLATOR OUTPUT BRIDGE CIRCUIT

Patent Number: Re. 34,879
Reissued: March 14, 1995
Assignee: Cardiac Pacemakers, Inc.

Reissue of
Patent Number: 4,998,531
Issued: March 12, 1991

Transmittal Letter For
Application for Patent Term Extension Under 35 USC §156 and 37 CFR §1.740

Assistant Commissioner for Patents
Box Patent Ext.
Washington, DC 20231

Dear Sir:

Enclosed is an original and four photocopies of an application for patent term extension.

The application is submitted by Cardiac Pacemakers, Inc., assignee of US Patent Re. 34,879 and holder of the regulatory approval granted with respect to the regulatory review period creating the eligibility for extension of the term of US Patent Re. 34,879. I am authorized to act on behalf of Cardiac Pacemakers, Inc. in this regard.

Please charge the $1,030 fee under 37 CFR §1.20(j), along with any underpayment, and credit any overpayment, to Deposit Account 03-0667.

If you have any questions, please contact me at your convenience.

Very truly yours,

Peter Forrest
Registration Number 33,235
Assistant Secretary of Cardiac Pacemakers, Inc.

May 5, 1995

CARDIAC PACEMAKERS, INC.
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Patent Number: Re. 34,879
Reissued: March 14, 1995
Assignee: Cardiac Pacemakers, Inc.

Reissue of
Patent Number: 4,998,531
Issued: March 12, 1991

Application for Patent Term Extension Under 35 USC §156 and 37 CFR §1.740

Assistant Commissioner for Patents
Box Patent Ext.
Washington, DC 20231

Dear Sir:

Please extend the term of US Patent Re. 34,879 under 35 USC §156 by a total of 363 days. The following information, numbered according to like numbered sub-sections of 37 CFR §1.740(a), supports this request.

(1) **The Approved Product**

The approved product is the CPI® Ventak® P2 AICD™ System, an implantable cardioverter defibrillator and ventricular pacing system manufactured by Cardiac Pacemakers, Inc. (CPI). The system primarily comprises an implantable Ventak® P2 Model 1620 or Model 1625 Pulse Generator, an external Handheld Programmer System (programmer) Model 2035, a Software Module (programmer software) Model 2835, and an accessory telemetry wand. (The system is designed for use with a variety of cardiac leads along with ancillary accessories such as lead adapters, wrenches, magnets, electrical cables, *etc.*, none of which were subject to the specific regulatory review at issue.) The system detects and terminates ventricular tachycardia and ventricular fibrillation, and provides pacing for bradycardia.

The pulse generators are multimodal treatment systems for patients with serious or potentially serious ventricular arrhythmias. In addition to delivering monophasic or biphasic shocks for terminating malignant arrhythmias, bradycardia pacing is available for bradycardia as well as to support the cardiac rhythm after defibrillation shock therapy. Programmable parameter settings allow adjustment of therapy to meet patient needs.

The Ventak® P2 Model 1620 and 1625 Pulse Generators differ slightly in volume and mass due primarily to different connection ports for the electrode leads. Specifically, the Ventak® P2 Model 1620 Pulse Generator has two 3.2mm defibrillation lead ports and one 3.2mm inline bipolar rate-sensing/pacing lead port. The Ventak® P2 Model 1625 Pulse Generator has two 6.1mm defibrillation

lead ports and two 4.75mm rate-sensing/pacing lead ports. These differences are not relevant to the reading of the claims of US Patent Re. 34,879 on either model of pulse generator, and thus both models are considered to be one product for purposes of regulatory review under the FFDCA as well as the scope and term of US Patent Re. 34,879.

The Handheld Programmer Model 2035 programmer system, when loaded with software from the Software Module Model 2835, communicates with the Ventak® P2 Model 1620 and Model 1625 Pulse Generators to: program therapy parameters for the implanted pulse generator; interrogate the programmed pulse generator; monitor and analyze patient data, and evaluate alternative prescription modes; store patient data that can be recalled later for analysis; generate printed reports that detail pulse generator functions, stored patient data, and test results; perform noninvasive diagnostic tests in an electrophysiology laboratory, operating room, emergency room, or at a patient's beside; and perform system maintenance and provide system diagnostic data.

(2) **The Federal Statute under which Regulatory Review Occurred**

The US Food and Drug Administration (FDA) reviewed the CPI® Ventak® P2 AICD™ System under Section 515 of the Federal Food, Drug and Cosmetic Act (FFDCA).

(3) **The Date on which the Product Received Permission for Commercial Marketing**

The FDA approved the CPI® Ventak® P2 AICD™ System under Section 515 of the FFDCA on March 10, 1995.

(4) **The Active Ingredient of a Drug Product**

Not applicable.

(5) **Timely Filing of this Application**

This application is being submitted within the sixty day period set forth in 37 CFR §1.720(f). The product was approved for commercial marketing on Friday, March 10, 1995, the 69th day of 1995. The last date on which this application could be filed is Tuesday, May 9, 1995, the 129th (69+60) day of 1995.

(6) **The Patent**

US Patent Re. 34,879 was reissued March 14, 1995 in the names of David E. Bocchi, Jeffrey T. Laackman, and Stanley M. Bach, Jr.

The patent is a reissue of US Patent 4,998,531 issued March 12, 1991 in the names of the same inventors, which issued from Application Number 07/501,527 filed March 28, 1990. Thus, as of this date, the expiration date of the reissue patent is March 12, 2008. Effective June 8, 1995, the expiration date of the reissue patent will be March 28, 2010.

The patent was reissued to correct errors in the claims, and it is the reissued claims which read upon the product subject to regulatory approval for which term extension is sought.

(7) **Copy of the Patent**

A full copy of US Patent Re. 34,879 is enclosed.

(8) **Disclaimers/Corrections/Maintenance Fee Receipts**

No disclaimer of the original patent or reissue patent was filed. No certificate of correction to the original patent or reissue patent was filed. A copy of the Maintenance Fee Receipt for the only maintenance fee due to date is enclosed. No reexamination certificate has been issued for the original patent or the reissue patent.

(9) **The Approved Product and the Patent**

US Patent Re. 34,879 claims the CPI® Ventak® P2 AICD™ System, and the method of using the system, in all five claims of the patent as identified below. Support for these statements may be found in the enclosed relevant selections from CPI document number 800128 entitled "SYST SCHEMATIC, VENTAK P2, MODEL 1620/1625," revision A, page 2 of 2; and CPI document number 530177 entitled "REQT, HYB, DEFIB OUTPUT MODULE," revision D, pages 4-8 and 11-19 of 29 (individually and collectively, the "design documents"). Please note that portions of the design documents (including but not limited to component manufacturer part and/or identification numbers) have been covered to maintain the confidentiality of information not necessary to support this showing. Sections of pages which have been so covered are indicated with a light blue "CONFIDENTIAL" label.

Claim 1 The Ventak® P2 AICD™ System includes an implantable pulse generator which comprises a pair (in series) of 250μF capacitors designated C1 and C2 in the design documents and C3 in the patent which store charge (at a predetermined voltage) and

are connected to an output module by pins designated HIV1 and HIV2 in the design documents, and VCAP in the patent.

Within the output module lie two IGBT power transistors each designated as Q401 (Q1 and Q12 in the patent), connected to pins HIV1 and HIV2 and capable of being triggered to active conditions by externally controlled gate inputs (described in more detail with respect to claim 2, below). The other side of the IGBT power transistors are connected to pins DFP and DFN which in turn are connected to the defibrillation electrodes DEFIB(-) and DEFIB(+) outside the output module.

Returning to the inside of the output module, the output bridge circuit also comprises [connected] ground return terminals identified as GND RTN in the patent and GNDP1 and GNDP2 in the design documents. The ground return terminals are selectively connected to the IGBT power transistors Q401 by a second pair of IGBT power transistors each designated as Q402 (corresponding to **Q2** and **Q13** in the patent).

Various ancillary components,. *e.g.* rectifier diodes, transistors, *etc.*, are shown in both the design documents and the patent. These components are present for steering purposes, transient protection, *etc.* but are not particularly relevant to the scope of the patent claims or the showing required by 37 CFR §1.740(a)(9).
The components of the output module are arranged in essentially identical and symmetric configurations, one for each of outputs DFP and DFN, designated as side A (for DFP) and side B (for DFN) in the design documents, and **12A** (for PATCH +) and **12B** (for PATCH -), respectively, in the patent.

The capacitor discharges through the IGBT transistors Q401 and thus across the defibrillation electrodes with either a positive polarity (*i.e.*, from DFP to DFN) or a negative polarity depending upon the arrangement of the two IGBT transistors Q401 as triggered by the two IGBT transistors Q402.

Claim 2

The Ventak® P2 AICD™ System further comprises two transformer-isolated gate driver circuits external to the output module (not shown in the design documents), each connected to a Q401 IGBT inputs (through pins SW1G/SW1S and SW2G/SW2S, respectively). External logic (not shown in the design documents) delivers to each gate driver circuit either a +12 volt or -12 volt pulse to turn on, or off, respectively, the Q401 IGBT to which it is connected by delivering a corresponding +12V or -12V

output to the gate-emitter capacitance of Q401 thereby triggering the Q401 to active condition or shorting the gate-emitter capacitance through a low impedance path.

Claim 3 The Ventak® P2 AICD™ System is an implantable defibrillation system for delivering monophasic and biphasic (a species of multiphasic) defibrillation pulses to a heart via a pair of electrodes implanted on or about the heart (identified as electrodes 22 and 24 in the patent) which are also connected to the system (at locations DEFIB(-) and DEFIB(+), respectively, in the design documents). The Ventak® P2 Model 1620 and 1625 Pulse Generators have the hardware for delivering higher-order multiphasic (*e.g.*, triphasic and quadraphasic) pulses and sequential defibrillation pulses, but the software to program the parameters of such pulses is not implemented in the Software Module Model 2835. The Ventak® P2 Model 1620 and 1625 Pulse Generators comprise an output circuit as described above for claim 1. The defibrillation electrode lead terminals are connected to the output bridge circuit by leads identified as PATCH + and PATCH -, corresponding to leads DFN and DFP, respectively, in the design documents. In other respects of the claim, see above for claims 1 and 2.

Claim 4 The Ventak® P2 AICD™ System generates multiphasic defibrillation pulses by charging a capacitor to a predetermined voltage and delivering the defibrillation pulses via four independently controlled switching elements operating as described above for claim 1.

Claim 5 When implanted according to FDA approved indications and manufacturer's instructions, the Ventak® P2 AICD™ System includes sensing electrodes mounted on or about the heart [sensing electrodes 20 in the patent] which are connected to the Ventak® P2 Model 1620 and 1625 Pulse Generators [at locations P/S(+) and P/S(-) in the design documents] to provide sensing and detection of arrhythmias of the heart, treating such arrhythmias as described above for claim 1.

(10) **Relevant Dates and Other Information**

The holder of the regulatory approval for the CPI® Ventak® P2 AICD™ System is Cardiac Pacemakers, Inc. (CPI),assignee of record of US Patent Re. 34,879.

Under 37 CFR §1.740(a)(10)(v), the following events and dates are applicable to the regulatory review and approval sought and granted to CPI for the Ventak® P2 AICD™ System. (37 CFR §1.740(a)(10)(i-iv) are not applicable.)

Effective Date of Investigational Device Exemption (IDE): December 20, 1991
(Note that this is the date of conditional approval)

IDE Number: G910178

Date of Pre-Market Approval Application (PMAA): August 30, 1993
(Note that the Application was in the form of a Supplement to PMAA 890061)

Number of PMAA: P930035
(Note that the Application was originally designated as P890061 Sup 007)

Date of Approval of PMAA: March 10, 1995

(11) Significant Activities

A partial listing of key events and mailing dates of correspondence between Cardiac Pacemakers, Inc. and the Food and Drug Administration (FDA) during the regulatory review period appears below. The number and frequency of events clearly establishes that, during the entire regulatory review period, Cardiac Pacemakers, Inc. continuously and diligently pursued approval by the FDA under the FFDCA to commercially distribute the CPI® Ventak® P2 AICD™ System.

Investigational Device Exemption (IDE) Phase

Application	October 7, 1991
Disapproval	November 6, 1991
First Amendment	November 22, 1991
Conditional Approval	December 20, 1991
Progress Report	January 30, 1992
Submission of Additional Information	February 1, 1992
Supplement; Request for Expansion of Study	February 6, 1992
Supplement	February 14, 1992
Approval of IDE Application	February 26, 1992
Submission of Additional Information	February 27, 1992
Disapproval of Supplement	March 6, 1992
Disapproval of Supplement	March 19, 1992
Supplement	April 10, 1992
Supplement	April 16, 1992
Supplement; Request for Expansion of Study	April 24, 1992
Conditional Approval of Supplement	May 14, 1992
Disapproval of Supplement	May 15, 1992
Disapproval of Supplement	May 27, 1992
Supplement	June 3, 1992
Supplement	June 24, 1992
Supplement	June 26, 1992
Conditional Approval of Supplement	July 2, 1992
Conditional Approval of Supplement	July 24, 1992
Conditional Approval of Supplement	July 29, 1992
Supplement	August 14, 1992
Supplement	August 21, 1992

Investigational Device Exemption (IDE) Phase, continued

Supplement	September 8, 1992
Approval of Supplement	September 16, 1992
Supplement	November 13, 1992
Conditional Approval of Supplement	December 16, 1992
Progress Report	December 23, 1992
Supplement	January 23, 1993
Conditional Approval of Supplement	February 23, 1993
Supplement	March 15, 1993
Supplement	April 5, 1993
Supplement	April 21, 1993
Disapproval of Supplement	May 6, 1993
Approval of Supplement	May 7, 1993
Supplement	May 21, 1993
Supplement	June 11, 1993
Approval of Supplement	June 14, 1993
Progress Report	June 16, 1993
Approval of Supplement	July 14, 1993
Request for Additional Information	July 16, 1993
Submission of Additional Information	August 27, 1993
Supplement	September 1, 1993
Supplement	October 1, 1993
Approval of Supplement	October 1, 1993
Supplement	October 18, 1993
Disapproval of Supplement	November 3, 1993
Supplement	December 3, 1993
Progress Report	December 16, 1993
Conditional Approval of Supplement	January 5, 1994
Supplement	January 18, 1994
Supplement	February 10, 1994
Supplement	February 24, 1994
Disapproval of Supplement	February 28, 1994
Approval of Supplements	March 4, 1994
Conditional Approval of Supplement	March 30, 1994
Supplement	April 15, 1994
Supplement	May 10, 1994

Investigational Device Exemption (IDE) Phase, continued

Approval of Supplements	May 17, 1994
Conditional Approval of Supplements	June 10, 1994
Supplement	July 26, 1994
Approval of Supplement	August 26, 1994
Progress Report	November 14, 1994
Conditional Approval of Supplements	December 15, 1994
Submission of Investigator Listing	December 21, 1994
Supplement	January 4, 1995
Supplement	January 6, 1995
Approval of Supplements	February 3, 1995
Approval of Supplements	February 9, 1995

Pre-Market Approval Application (PMAA) Phase

Application	August 30, 1993
Acknowledgment of Application	August 31, 1993
Correction of PMA Number	October 14, 1993
Threshold Determination	December 6, 1993
Amendment	December 22, 1993
Request for Information	April 18, 1994
Amendment	June 21, 1994
Meeting	July 6, 1994
Response to Discussions in Meeting	July 14, 1994
Notice of Deficiencies	August 24, 1994
Amendment	September 13, 1994
Amendment	September 22, 1994
Draft Response; Meeting Notes; Proposed Review Timeline; Replacement Pages	October 11, 1994
Amendment	October 14, 1994
Amendment	November 18, 1994
[Other Activity; See Below]	November 19, 1994 to March 9, 1995
Approval of PMAA	March 10, 1995

Please note that correspondence and other activity did occur between November 19, 1994 and March 9, 1994 but is not recorded here due only to temporary clerical backlog. Further evidence of such activity is available upon request.

(12) Eligibility for and Calculation of Extension

In my opinion, US Patent Re. 34,879 is eligible for an extension of patent term under 35 USC §156 in the amount of 363 days, as set forth below.

(a) Eligibility for extension under 35 USC §156

(1) This application is being submitted prior to the expiration of US Patent Re. 34,879 on March 12, 2008. (Effective June 8, 1995, the expiration date of US Patent Re. 34,979 will be March 28, 2010.)

(2) US Patent Re. 34,879 has never had an extension of patent term.

(3) This application is submitted by Cardiac Pacemakers, Inc., the assignee of record of US Patent Re. 34,879 and US Patent 4,998,531 by virtue of an assignment recorded on March 28, 1990 at reel 5273, frames 531-535 in the records of the United States Patent and Trademark Office. I am an officer of Cardiac Pacemakers, Inc. and am authorized to conduct all business in the United States Patent and Trademark Office on behalf of Cardiac Pacemakers, Inc. If required, proof of my specific authority to submit this application, in accordance with 35 USC §156(d) and 37 CFR §1.740(b)(1), will be provided in response to an order to show cause why the USPTO should not deny this application under 35 USC §156(c)(3) and 37 CFR §1.730; or by way of petition under 37 CFR §1.181, §1.182, or §1.183, all as provided by 37 CFR §1.740(c).

(4) The product was subject to regulatory review by the US Food and Drug Administration (FDA) under Section 515 of the Federal Food, Drug and Cosmetic Act (FFDCA).

(5) The permission for commercial marketing under Section 515 of the FFDCA was the first permission for commercial marketing for the product.

(b) Calculation of Length of Extension

US Patent Re. 34,879 issued on October 4, 1983, after the September 24, 1984 date of enactment, as defined in 35 USC §(f)(7), of the statute now codified at 35 USC §156. Thus, under 35 USC 156(g)(6)(A), the total possible term extension is five years, or 1825 days.

The period beginning on the date a clinical investigation on humans involving the product was begun, *i.e.*, the date the Application for Investigational Device Exemption (IDE) was

conditionally accepted (December 20, 1991), and ending on the date the Pre-Market Approval Application (PMAA) was filed (August 30, 1993), is 619 days (including the leap day of February 29, 1992).

The period beginning on the date the PMAA was filed (August 30, 1993), and ending on the date the product was approved for commercial marketing (March 10, 1995), is 557 days.

The sum of the two periods above is 1176 days.

US Patent Re. 34,879 is based on US Patent 4,998,531 which issued on March 12, 1991, before clinical investigation on humans involving the product began on December 20, 1991, and thus the regulatory review period is not reduced under the main clause of 35 USC §156(c).

Cardiac Pacemakers, Inc. continuously and diligently worked to secure acceptance of the PMAA by the FDA during the entire period of regulatory review. Therefore, no reduction for lack of diligence should be made under 35 USC §156 (c)(1) or 37 CFR §1.777(d)(1)(ii).

One-half of the period beginning on the date the IDE was conditionally accepted (December 20, 1991), and ending on the date the PMAA was filed (August 30, 1993), is one-half of 619 days, or 309 days. Under 35 USC §156 (c)(2), this amount is subtracted from the length of the regulatory review period. The difference is 1176 days minus 309 days, or 867 days.

As of the date of commercial approval of the product, March 10, 1995, the patent term remaining (to March 12, 2008) was 13 years, two days. The sum of this amount and the reduced regulatory period of 867 days (2.4 years), is 15.4 years, more than the maximum 14 year extended term permitted by 35 USC §156(c)(3) and 37 CFR §1.777(d)(2-4). Thus, the reduced regulatory period is reduced further to 363 days to provide a maximum extended term of not greater than 14 years.

Therefore, US Patent Re. 34,879 is eligible for an extension of term of 363 days.

(13) **Duty of Disclosure**

I acknowledge my duty to disclose to the Commissioner of Patents and Trademarks and the Secretary of Health and Human Services any information which is material to the determination of entitlement to the extension of patent term of US Patent Re. 34,879. I specifically acknowledge the requirements of 37 CFR §1.765.

In this regard, please note two particular issues:

(1) Extensions of patent term have been previously granted for patents which may also read on the CPI® Ventak® P2 AICD™ System; and US Patent Re. 34,879 may also read on other products which have undergone regulatory review such that other patents on such other products were granted extensions of term.

Specifically, patent term extensions have been granted previously for:

- US Patent B1 Re. 27,757 (a reissue of US Patent 3,614,955, as reflected by Reexamination Certificate Number 638 issued March 10, 1987), based upon regulatory review of implantable defibrillators known as the AID® Model B and AID® Model BR; this patent (now expired) is believed to read on the CPI® Ventak® P2 AICD™ System. US Patent Re. 34,879 is not believed to read on the AID® Model B or Model BR.

- US Patent 4,316,472, based upon regulatory review of an implantable cardioverter defibrillator known as Ventak® P Model 1600, certain claims of which patent also read on certain implantable cardioverter/defibrillators which did not require regulatory review as defined by 35 USC §156(g), specifically those known as Ventak® Model 1550 and Ventak® Model 1555; this patent is believed to read on the Ventak® P2 AICD™ System. US Patent Re. 34,879 is not believed to read on the Ventak® P Model 1600, the Ventak® Model 1550, or the Ventak® Model 1555.

- US Patent 4,868,908, based on regulatory review of an implantable cardioverter defibrillator pacer known as Ventritex® Cadence® Tiered Therapy Defibrillator System Model V-100; it is not known if this patent reads on the CPI® Ventak® P2 AICD™ System. US Patent Re. 34,879 is believed to read on the Ventritex® Cadence® Tiered Therapy Defibrillator System Model V-100.

- US Patent 4,052,991, based upon regulatory review of an implantable cardioverter defibrillator pacer known as Medtronic® PCD® Tachyarrhythmia Control Device Model 7217B; it is not believed that this patent reads on the CPI® Ventak® P2 AICD™ System. It is not known if US Patent Re. 34,879 reads on the Medtronic® PCD® Tachyarrhythmia Control Device Model 7217B.

In addition, an application for patent term extension is currently pending for:

- US Patent 4,407,288, based upon regulatory review of an implantable cardioverter defibrillator pacer system known as CPI® Ventak® PRx® AICD™ System; this patent is not believed to read on the CPI® Ventak® P2 AICD™ System, but it is believed to read on the Ventritex® Cadence® Tiered Therapy Defibrillator System Model V-100 and the Medtronic® PCD® Tachyarrhythmia Control Device Model 7217B.

(2) Mr. Gerald Dost of the USPTO and I discussed this application on May 4, 1995. The specific context discussed was the proper procedure for submission of trade secret and proprietary materials in support of this application. While MPEP §724 discusses such submissions in the context of patent applications and reexamination proceedings, Mr. Dost indicated that the general procedures outlined in MPEP §724 should not be followed because of public access to patent term extension files. Mr. Dost also indicated that it was permissible to cover portions of the enclosed materials not relevant to the claims of US Patent Re. 34,879, as done in this application, provided that an adequate showing under 37 CFR §1.740(a)(9) was made. I understand that Mr. Dost's advice was informal and does not substitute for formal review of this application.

(14) **Fee**

As noted in the letter of transmittal, please charge the $1,030 fee under 37 CFR §1.20(j) to Deposit Account 03-0667. Please also charge any other fee necessary to process this application to Deposit Account 03-0667.

(15) **Notice**

Please address all inquiries and correspondence regarding this application to:

Peter Forrest
Mail Stop A390
Cardiac Pacemakers, Inc.
4100 Hamline Avenue North
St. Paul, MN 55112-5798

Please address all telephone calls to Peter Forrest at (612) 582-4400.

(16) **Duplicate Papers**

Please find enclosed one original and four complete duplicates of this application and all exhibits. One duplicate is required by 37 CFR §1.740(a)(16), and three additional duplicates provided for the convenience of the USPTO. I certify as a registered practitioner that all duplicates are true and accurate photocopies of the original.

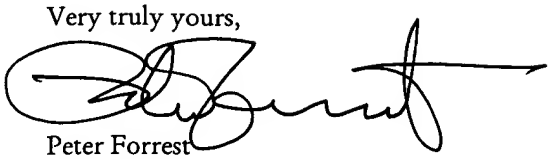
(17) **Declaration**

I am an attorney authorized to practice before the United States Patent and Trademark Office. I have reviewed and I understand the contents of this application. I believe that US Patent Re. 34,879 is subject to extension pursuant to 37 CFR §1.710. I believe that an extension of 363 days is justified under 35 USC §156 and applicable regulations. I believe that US Patent Re. 34,879 meets the conditions for extension of term as set forth in 37 CFR §1.720.

All statements in this application made of my own knowledge are true, and all statements in this application made on information and belief I believe to be true. I make these statements knowing that willful false statements and the like may be punished by fine or imprisonment or both under Section 1001 of Title 18 of the United States Code, and that such willful false statements may also jeopardize this application for extension of the patent term of US Patent Re. 34,879.

If you have any questions, please contact me at your convenience.

Very truly yours,



Peter Forrest
Registration Number 33,235
Assistant Secretary of Cardiac Pacemakers, Inc.

May 5, 1995

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US00RE34879E

United States Patent [19]

Bocchi et al.

[11] E Patent Number: Re. 34,879

[45] Reissued Date of Patent: Mar. 14, 1995

[54] **IMPLANTABLE N-PHASIC DEFIBRILLATOR OUTPUT BRIDGE CIRCUIT**

[75] Inventors: **David E. Bocchi**, Vadnais Heights; **Jeffrey T. Laackman**, Isanti; **Stanley M. Bach, Jr.**, Shoreview, all of Minn.

[73] Assignee: **Cardiac Pacemakers, Inc.**, St. Paul, Minn.

[21] Appl. No.: **51,899**

[22] Filed: **Mar. 12, 1993**

Related U.S. Patent Documents

Reissue of:

[64] Patent No.: **4,998,531**
Issued: **Mar. 12, 1991**
Appl. No.: **501,527**
Filed: **Mar. 28, 1990**

[51] **Int. Cl.**[6] **A61N 1/39**
[52] **U.S. Cl.** **607/5**
[58] **Field of Search** 607/4, 5, 6, 7

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,504,773	3/1985	Suzuki et al. .
4,693,253	9/1987	Adams .
4,840,177	6/1989	Charbonnier et al. .
4,850,357	7/1989	Bach, Jr. .

Primary Examiner—William E. Kamm
Assistant Examiner—George Manuel
Attorney, Agent, or Firm—Keck, Mahin & Cate

[57] **ABSTRACT**

An output bridge circuit comprising four independently controlled transistors connected between first and second electrode terminals and a defibrillation capacitor. Two of the four transistors are driven by push-pull driver circuits and connected between the capacitor and the first and second electrode terminals. The remaining two transistors are connected between the first and second electrode terminals and ground terminals. By triggering one of the transistors connected to the push-pull driver circuits and one of the transistors connected between the electrode terminals and the ground terminal, a mono-phasic, multi-phasic, or sequential defibrillation pulse can be generated by activating the appropriate transistors.

5 Claims, 6 Drawing Sheets

3-12-91
17
08

3-28-90
20
10

95
17
112

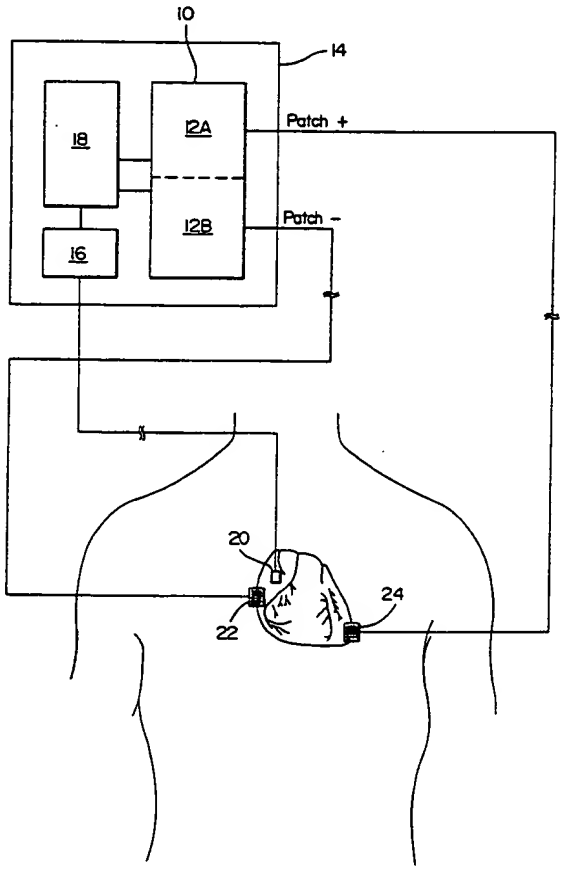
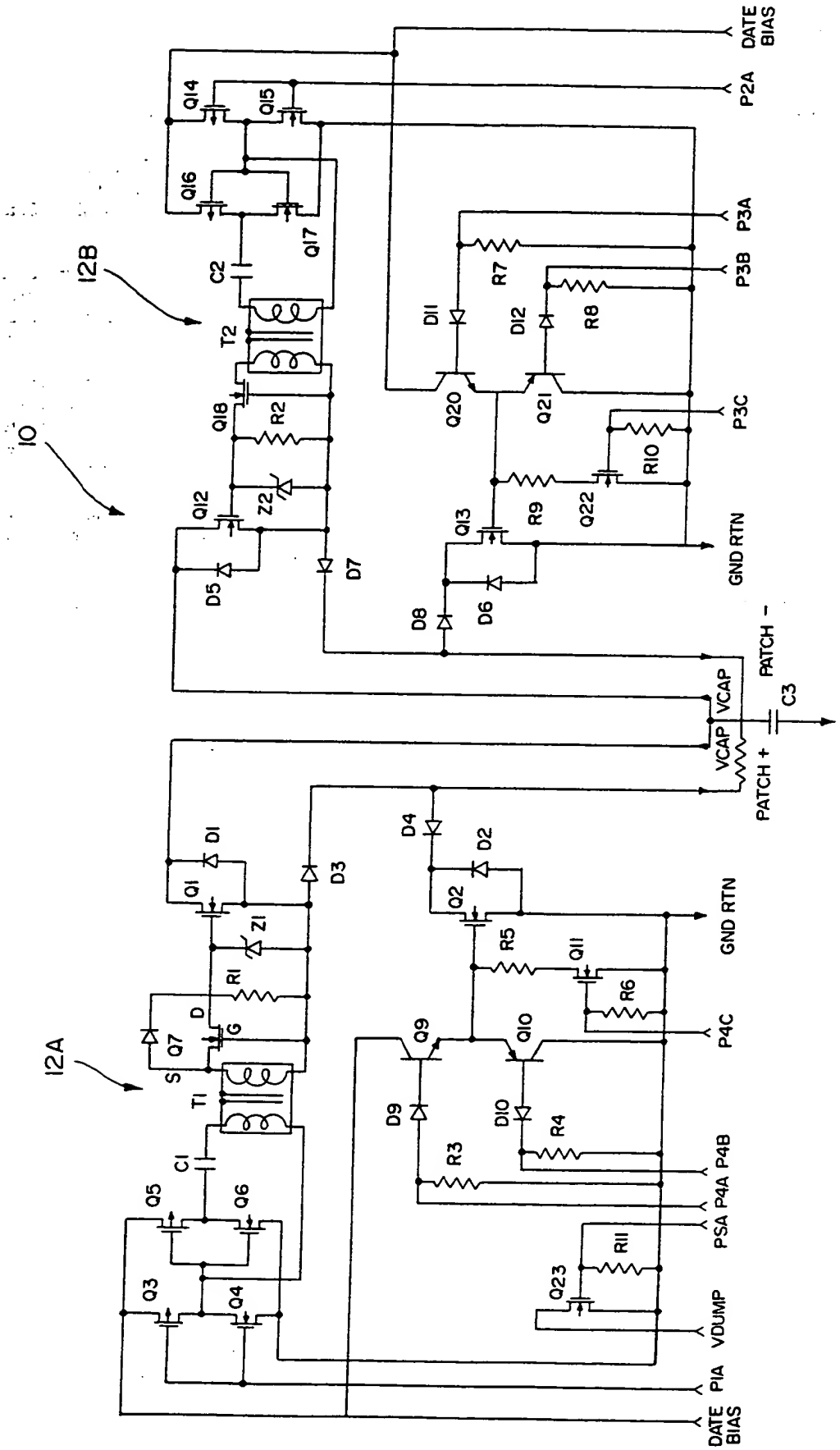


FIG. 1


DATE BIAS
P2A
Q14
Q15
Q16
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C2
12B
T2
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R2
10
Q12
Z2
D5
D7
P3A
P3B
R7
R8
D11
D12
Q20
Q21
P3C
R10
Q22
R9
Q13
GND RTN
D8
D6
PATCH -
VCAP
C3
VCAP
PATCH +
D1
Q1
Z1
R1
D
G
Q7
S
12A
T1
C1
Q5
Q6
Q3
Q4
D3
D4
D2
Q2
GND RTN
R5
Q11
R6
P4C
Q9
Q10
D9
D10
R4
R3
P4B
P4A
PSA
R11
Q23
VDUMP
PIA
DATE BIAS

FIG. 2

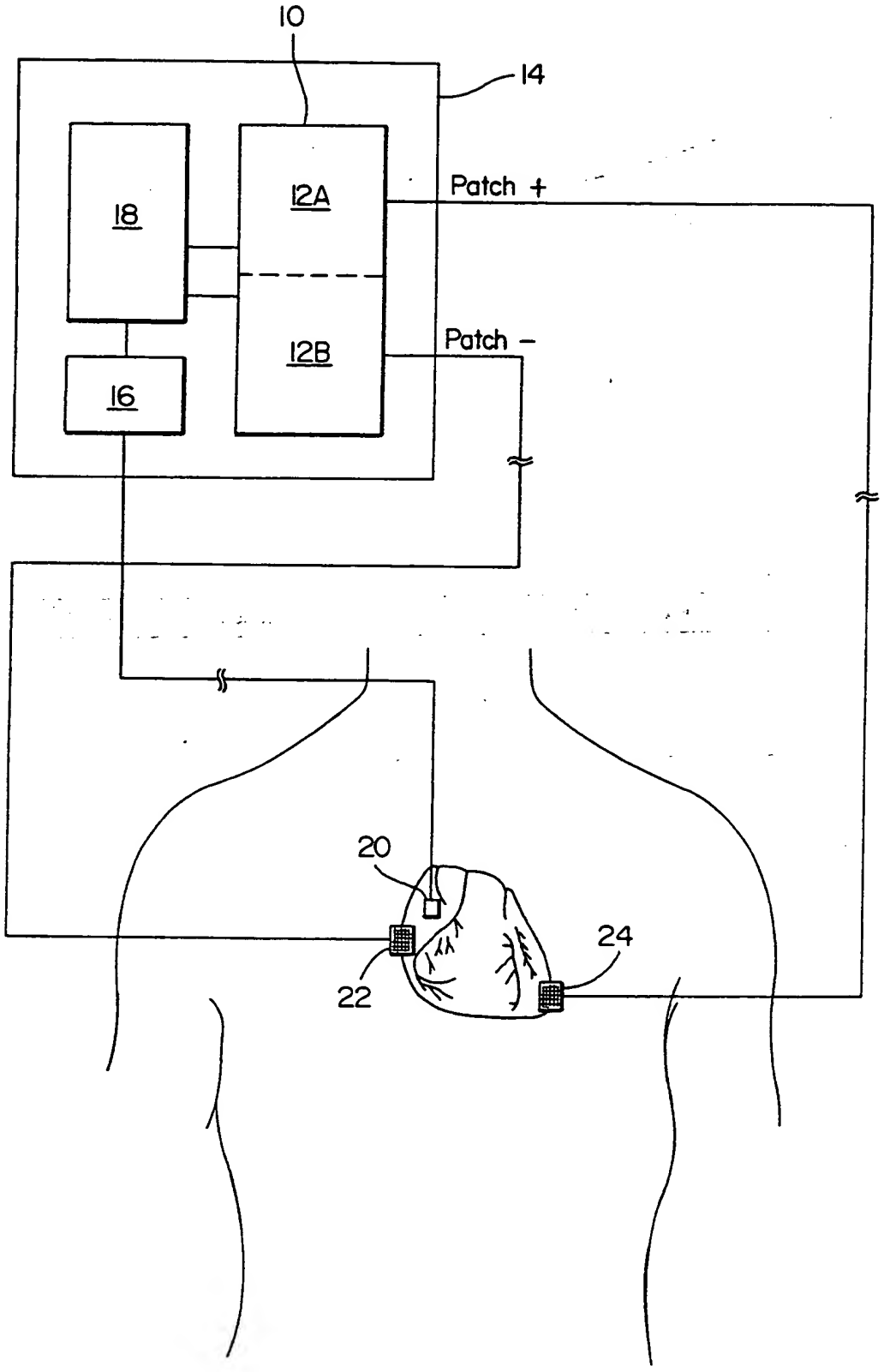


FIG. 3a

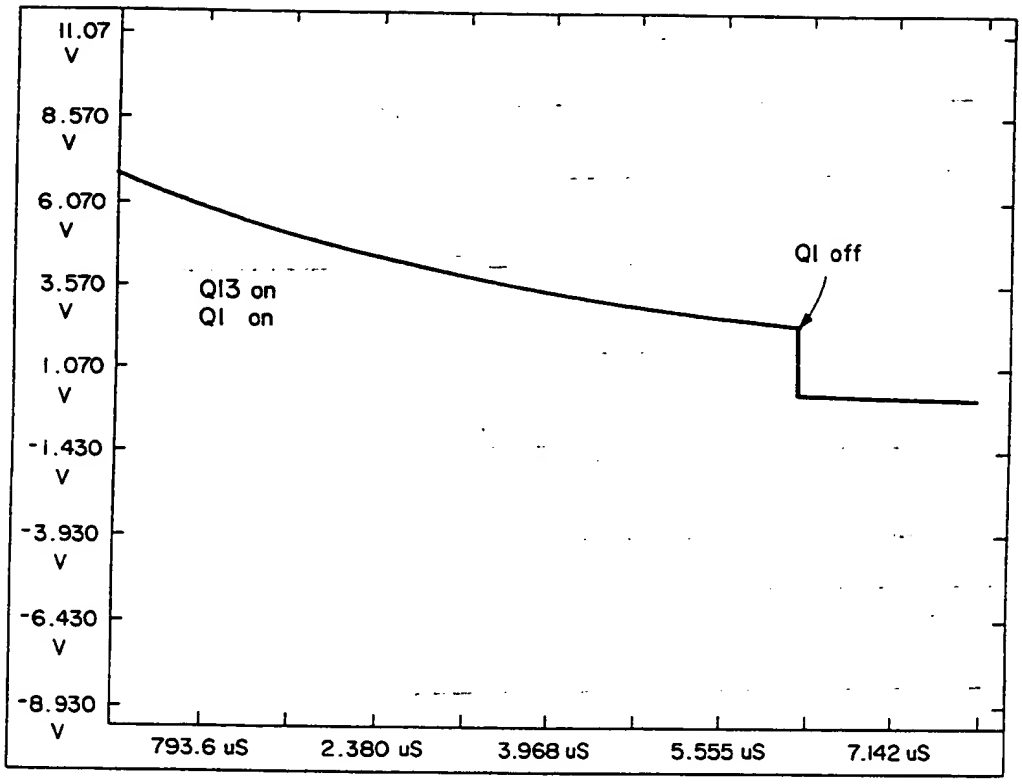

11.07 V
8.570 V
6.070 V
3.570 V
1.070 V
-1.430 V
-3.930 V
-6.430 V
-8.930 V
793.6 uS
2.380 uS
3.968 uS
5.555 uS
7.142 uS
Q13 on
Q1 on
Q1 off

FIG. 3b

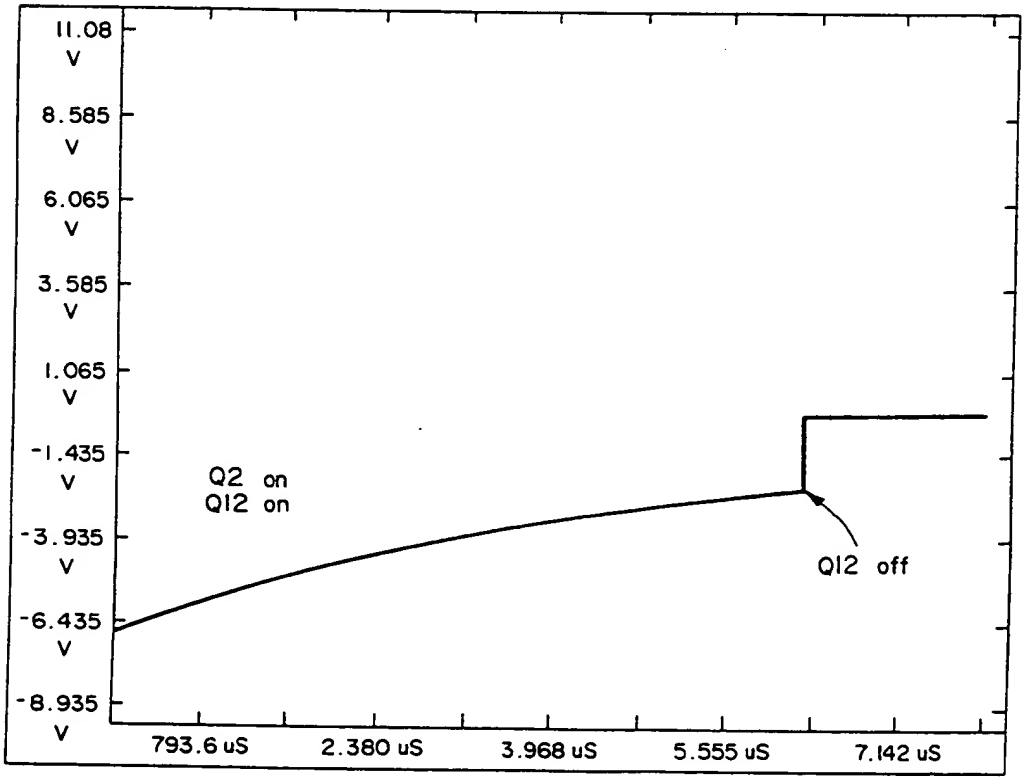

11.08 V
8.585 V
6.065 V
3.585 V
1.065 V
-1.435 V
-3.935 V
-6.435 V
-8.935 V
793.6 uS
2.380 uS
3.968 uS
5.555 uS
7.142 uS
Q2 on
Q12 on
Q12 off

FIG. 3c

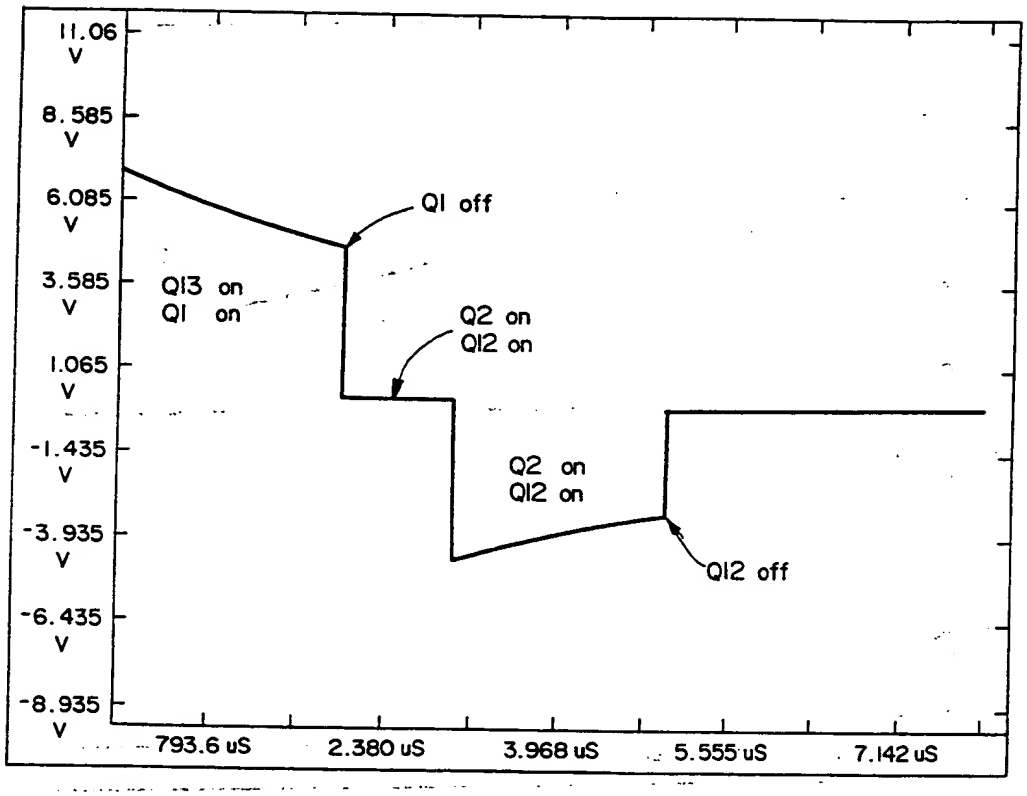

11.06 V
8.585 V
6.085 V
3.585 V
1.065 V
-1.435 V
-3.935 V
-6.435 V
-8.935 V
793.6 uS
2.380 uS
3.968 uS
5.555 uS
7.142 uS
Q1 off
Q13 on
Q1 on
Q2 on
Q12 on
Q2 on
Q12 on
Q12 off

FIG. 3d

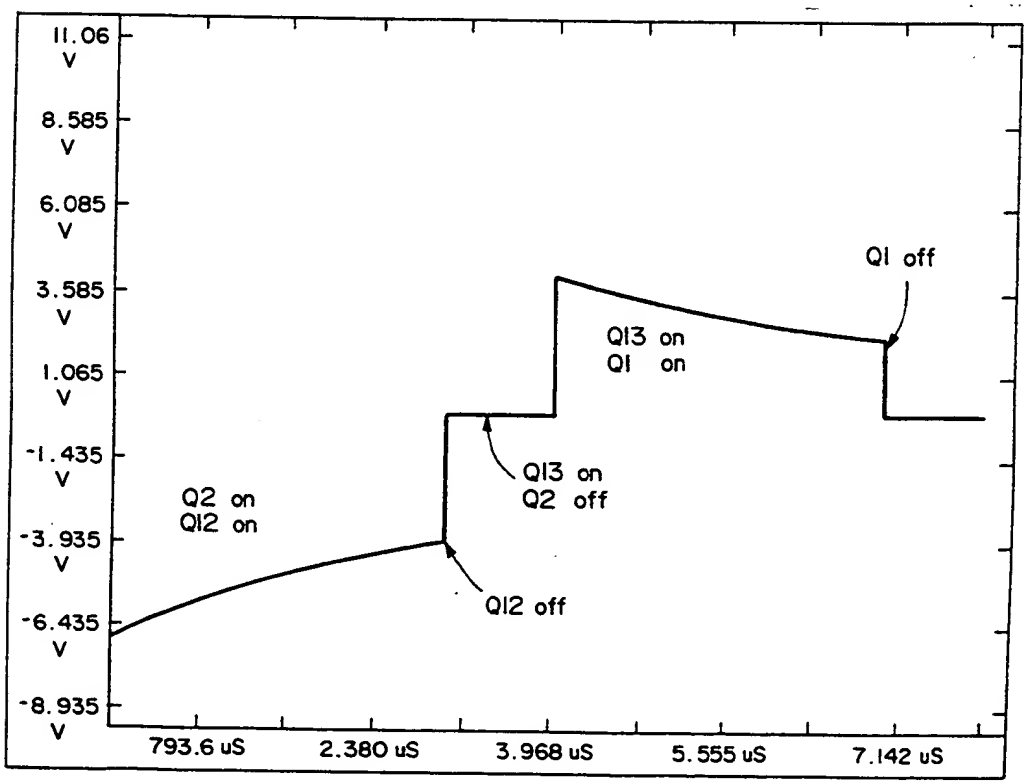

11.06 V
8.585 V
6.085 V
3.585 V
1.065 V
-1.435 V
-3.935 V
-6.435 V
-8.935 V
793.6 uS
2.380 uS
3.968 uS
5.555 uS
7.142 uS
Q1 off
Q13 on
Q1 on
Q13 on
Q2 off
Q2 on
Q12 on
Q12 off

FIG. 3e

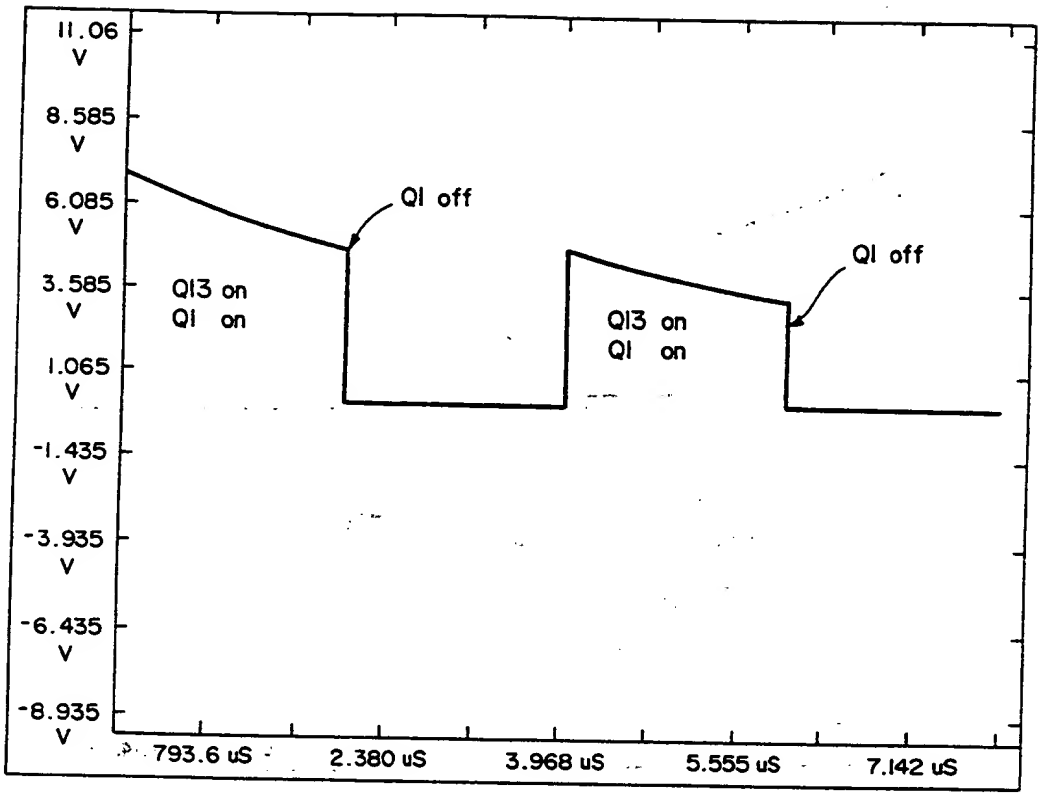

11.06 V
8.585 V
6.085 V
3.585 V
1.065 V
-1.435 V
-3.935 V
-6.435 V
-8.935 V
Q1 off
Q13 on
Q1 on
Q13 on
Q1 on
Q1 off
793.6 uS
2.380 uS
3.968 uS
5.555 uS
7.142 uS

FIG. 3f

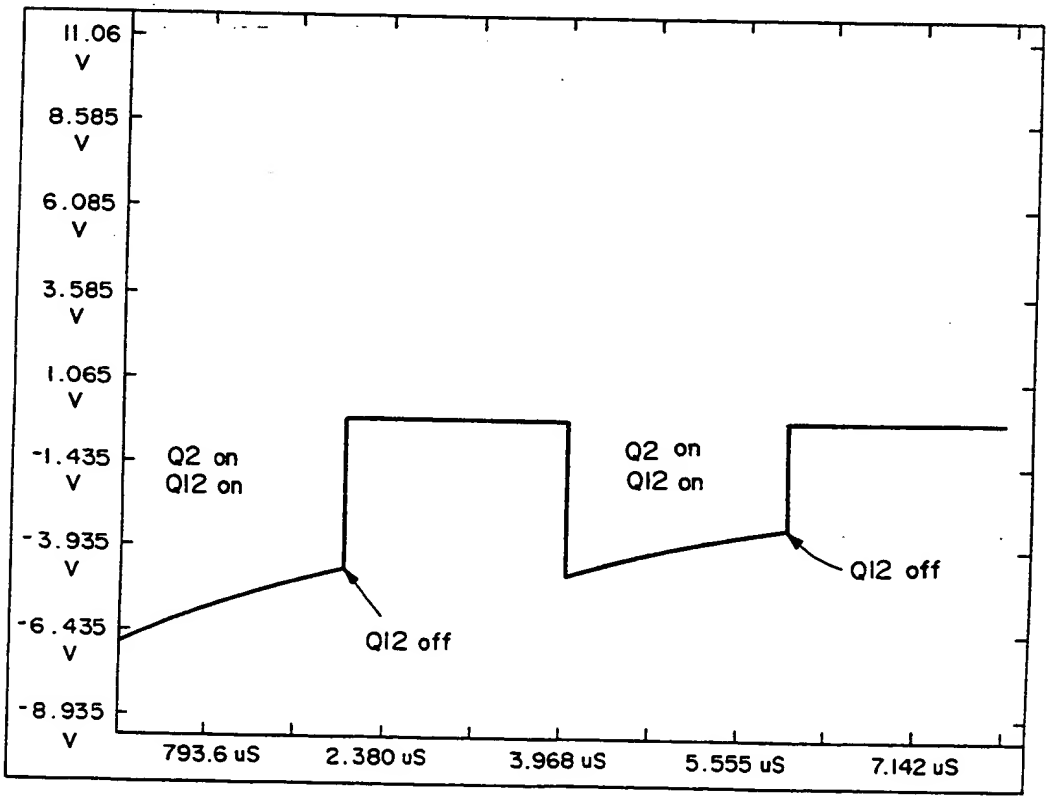
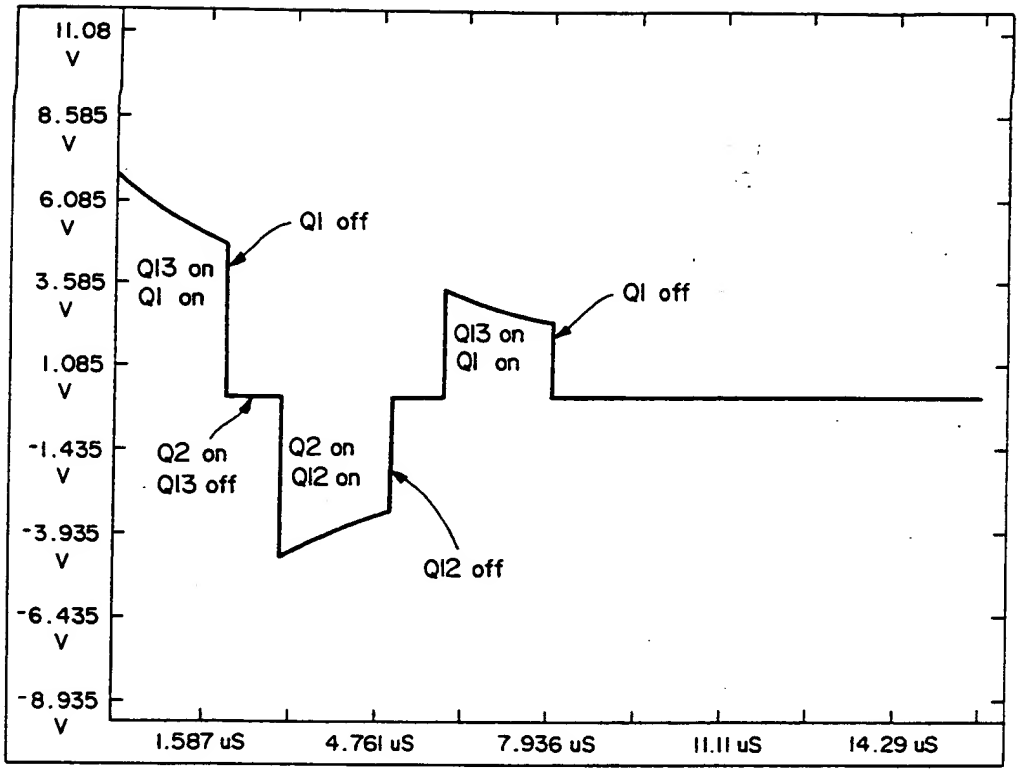

11.06 V
8.585 V
6.085 V
3.585 V
1.065 V
-1.435 V
-3.935 V
-6.435 V
-8.935 V
Q2 on
Q12 on
Q2 on
Q12 on
Q12 off
Q12 off
793.6 uS
2.380 uS
3.968 uS
5.555 uS
7.142 uS

FIG. 3g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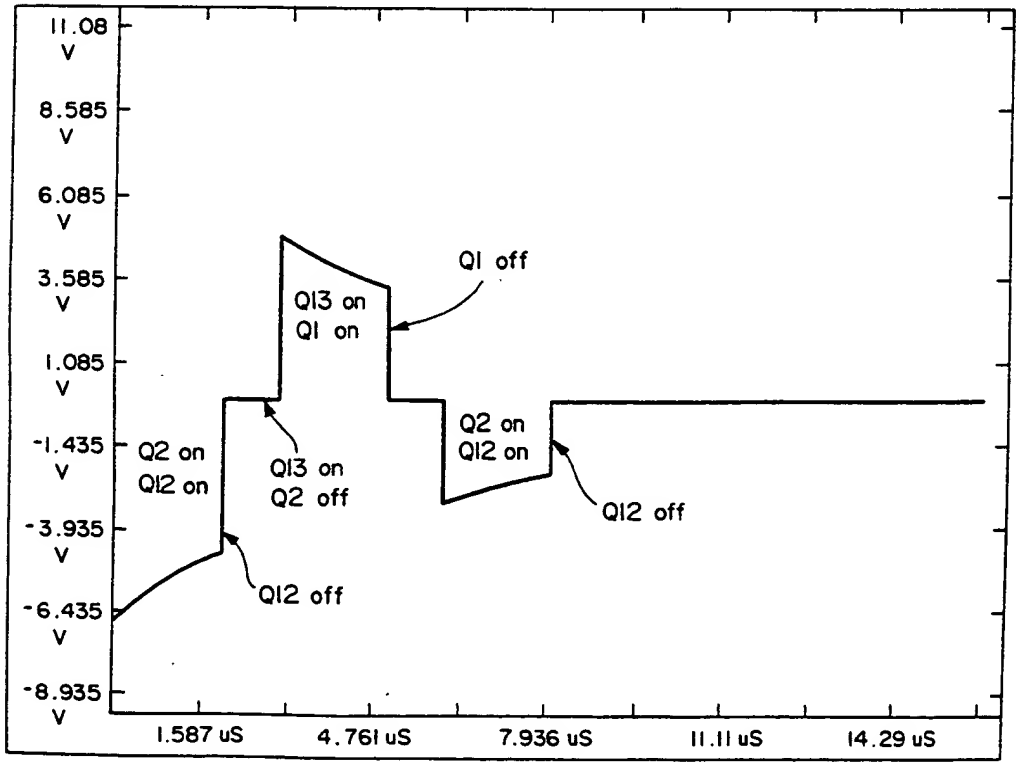
8.585 V
6.085 V
3.585 V
1.085 V
-1.435 V
-3.935 V
-6.435 V
-8.935 V
1.587 uS
4.761 uS
7.936 uS
11.11 uS
14.29 uS
Q1 off
Q13 on Q1 on
Q2 on Q13 off
Q2 on Q12 on
Q12 off
Q13 on Q1 on
Q1 off

FIG. 3h


11.08 V
8.585 V
6.085 V
3.585 V
1.085 V
-1.435 V
-3.935 V
-6.435 V
-8.935 V
1.587 uS
4.761 uS
7.936 uS
11.11 uS
14.29 uS
Q1 off
Q13 on Q1 on
Q2 on Q12 on
Q13 on Q2 off
Q12 off
Q2 on Q12 on
Q12 off

IMPLANTABLE N-PHASIC DEFIBRILLATOR OUTPUT BRIDGE CIRCUIT

Matter enclosed in heavy brackets [ ] appears in the original patent but forms no part of this reissue specification; matter printed in italics indicates the additions made by reissue.

BACKGROUND OF THE INVENTION

The present invention relates to an implantable defibrillator output circuit, and more specifically to an output bridge circuit for issuing mono-phasic, multi-phasic, and sequential defibrillation pulses.

In the field of implantable defibrillators, it has been found that a bi-phasic defibrillation pulse applied to a fibrillating heart is useful in controlling and arresting ventricular fibrillation. See for example, commonly assigned U.S. patent application Ser. No. 143,061, filed Jan. 12, 1988, and entitled BI-PHASIC PULSE GENERATOR FOR AN IMPLANTABLE DEFIBRILLATOR. This application discloses a circuit for generating a bi-phasic voltage pulse, the circuit including first and second thyristors for regulating the voltage of a capacitor. The circuit further includes an output sensing section for sensing the exponential decay of the capacitor and signalling a control circuit to switch metal oxide silicon insulated gate transistors (MOSIGT) in a ground circuit such that after one thyristor applies a voltage pulse to the heart in a first polarity the control circuit interrupts to turn off the thyristor. The other thyristor then applies the voltage pulse to the heart in a second and opposite polarity. It, in turn, is turned off by a second MOSIGT. While this disclosed circuit is capable of generating a bi-phasic defibrillation pulse, the ground return terminal needs to be disconnected in order to commutate the current flow through the electrodes to the heart.

SUMMARY OF THE INVENTION

It is a primary object of the present invention to provide an implantable defibrillator output circuit capable of delivering a multi-phasic defibrillation pulse without having to repeatedly disconnect the ground return reference terminal.

It is another object of this invention to provide an implantable defibrillator output bridge circuit wherein energy on a defibrillator capacitor can be used for the delivery of bi-phasic, tri-phasic, and sequential defibrillation pulses.

The present invention comprises an implantable defibrillator output circuit comprising a bridge configuration having four Metal Oxide Silicon Insulated Gate Transistors (MOSIGT's) and arranged with the top two transistors having transformer isolated gate drives and the bottom two transistors having turn off time control and low impedance clamping. Furthermore, all four MOSIGT's have independent on/off control to allow for mono-phasic, bi-phasic, tri-phasic, and sequential defibrillation pulses, and permit the selection of delivery polarity as either positive or negative without having to disconnect the ground return reference.

The above and other objects and advantages will become more readily apparent when reference is made to the following description taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an electrical schematic diagram of the implanatable defibrillator output bridge circuit in accordance with the present invention.

FIG. 2 is a schematic diagram illustrating the use of the implantable defibrillator output bridge circuit of the present invention in conjunction with an implanatable defibrillation system.

FIGS. 3a-3h are graphical plots of defibrillation pulses produced by the output bridge circuit illustrated in FIG. 1.

DETAILED DESCRIPTION OF THE DRAWINGS

Referring first to FIG. 1, the implantable defibrillator output bridge circuit is generally shown at **10**. The circuit **10** comprises a left portion **12a** and a right portion **12b**. With the exception of the transistor Q23 and resistor R11, the circuit portions **12a** and **12b** are mirror images of each other. Therefore, a detailed description of circuit portion **12a** will be made first and a brief description of circuit portion **12b** will follow.

The circuit **10** includes input signal pins P1A, P2A, P3A, P4A, P5A, P3B, P4B, P3C, and P4C. In addition, output pins are provided at patch+and patch−for connecting the circuit **10** to defibrillation electrodes implanted on the heart. Ground return pins are also provided for each side of the circuit **10**, the function of which will be described hereinafter. Each circuit portion **12a** and **12b** connects to a capacitor C3 at respective pins designated Vcap. The four MOSIGT's are transistors Q1, Q2, Q12, and Q13. The top transistors Q1 and Q12 have transformer isolated gate drives. The bottom transistors Q2 and Q13 have controlled turn off time and low impedance clamping. Each MOSIGT Q1, Q2, Q12, and Q13 has independent on/off control. As will become more apparent hereinafter, transistors Q1 and Q12 are used for controlling the multi-phasic nature of the defibrillation pulse, while transistors Q2 and Q13 set the polarity of the defibrillation pulse by selecting one of the pins patch+or patch−as the ground-return.

Input signal pin P1A connects to push-pull driver transistor configuration comprising transistors Q3, Q4, Q5, and Q6. The push-pull driver generates a square wave with amplitude +/−Gate-bias. The push-pull driver is connected to a DC blocking capacitor C1, which in turn is connected to the primary side of the pulse transformer T1. The gate and source of the transistor Q7 connects across the secondary side of the transformer T1 while the gate and drain of Q7 are connected in parallel with resistor R1 and zener diode Z1. The gate and source of the transistor Q1 are connected in parallel with resistor R1 and zener diode Z1. Diode D1 connects across the drain and source of the transistor Q1.

Diodes D3 and D4 connect the source of transistor Q1 to the drain of transistor Q2. Diode D2 connects across the source and drain of the transistor Q2. The gate of the transistor Q2 is connected to resistor R5 and the emitters of the transistors Q9 and Q10. Resistor R5 also connects to the drain of the transistor Q11. Connected across the gate and source of transistor Q11 is resistor R6.

A series connection of resistor R3 and diode D9 is connected to the base of the transistor Q9. Similarly, the series connection of resistor R4 and diode D10 is connected to the base of the transistor Q10. Input signal

pins P4A and P4B connect between resistor R3 and diode D9, and resistor R4 and diode D10, respectively. Transistors Q23 is provided with resistor R11 connected across its gate and source for providing access to an external dump load as will be explained hereinafter.

The circuit portion 12b is the same as circuit portion 12a with the exception of transistor Q23 and resistor R11. Transistors Q14, Q15, Q16, and Q17 comprise a push-pull driver configuration connected to the pulse transformer T2 in the same way as transistors Q3–Q6. Transistor Q18 is connected to the secondary side of the transformer T2 and to resistor R2, zener diode Z2, and transistor Q12, similar to the connections between transistor Q7, resistor R1, zener diode Z1 and transistor Q1 in circuit portion 12a.

Diodes D7 and D8 connect the transistor Q1 to the transistor Q13 in a similar manner as diodes D3 and D4 connect transistor Q1 to transistor Q2. The gate of transistor Q13 connects to the emitters of transistors Q20 and Q21 and to resistor R9. The series connection of resistor R7 and diode D11 is connected to the base of the transistor Q20. Similarly, the series connection of diode D12 and resistor R8 is connected to the base of transistor Q21. The input signal control pins P3A and P3B connect between resistor R7 and diode D11, and resistor R8 and diode D12, respectively. Resistor R9 connects the emitters of the transistors Q20 and Q21 to the drain of the transistor Q22. Resistor R10 is connected across the gate and source of transistor Q22.

The operation of circuit 10 will now be described with respect to the transistor Q1 and Q13 corresponding to input signal pins P1A, and P3A, P3B, and P3C, respectively, while pins P4A, P4B, P2A and P4C are at ground potential. The Gate-bias voltage is positive with respect to ground-return. To operate transistor Q1, a positive going pulse with respect to the ground-return is applied to pin P1A. This drives the push-pull driver configuration of transistors Q3–Q6 to generate a square wave with amplitude +/−Gate-bias. This drives the primary side of the pulse transformer T1 via the DC blocking capacitor C1. A positive pulse on the dotted secondary of the pulse transformer T1 causes the intrinsic body diode, created by making the gate more negative than the source, to conduct, which then causes the gate of transistor Q1 to charge to+Gate-bias volts, turning transistor Q1 on. As long as a positive voltage pulse is applied on pin P1A, transistor Q1 is on until the gate charge is depleted. A negative pulse on the secondary of pulse transformer T1 caused by pin P1A returning to ground potential forces the gate of the transistor Q7 to be more positive than the source of transistor Q7, so that transistor Q7 turns on providing a low impedance discharge path for the gate charge on transistor Q1. Hence, Q1 turns off. The zener diode Z1, when forward biased, prevents the gate of transistors Q1 from charging to −Gate-bias volts. The overall impedance that the gate of transistor Q1 sees when charging or discharging is the output impedance of the push-pull driver configuration of transistors Q3–Q6. Resistor R1 provides a high impedance gate discharge path, gate to source, of transistor Q1, that prevents charge from accumulating on the gate of transistor Q1 and therefore prevents false turn on. The zener diode Z1 clamps positive gate to source voltage of transistor Q1 in excess of positive gate-bias that may be caused via the transfer capacitance of transistor Q1 by rapidly changing positive drain to source voltages. Zener diode Z1 also clamps negative gate to source voltages in excess of a diode drop caused by the same conditions. Further, zener diode Z1 protects the gate to source potential of transistor Q1 from exceeding its maximum ratings and also helps to minimize false turn on caused by a change of voltage with respect to time seen by the drain to source of transistor Q1.

Diode D1 protects Q1 if the source potential is greater than drain potential. Diode D3 also protects Q1 in an effort to keep current from flowing into the source of Q1 if the cathode side of diode D3 becomes more positive than the drain of transistor Q1. This condition can occur due to the stray inductance and the counter EMF generated by the change in current with respect to time when the other side of the bridge is turned off. Diodes D6 and D8 protect transistor Q13 in the same way as diodes D1 and D3 protect transistor Q1.

To operate transistor Q13, input signal pins P3A, P3B, and P3C are employed. A positive going pulse with respect to ground-return on pins P3A and P3B turns on transistor Q20, and turns off transistor Q21, respectively, which then allows the gate of transistor Q13 to charge to+Gate-bias volts, thus turning transistor Q13 on. The input signal at pin P3C must be kept low to keep transistor Q13 on. When pin P3A is set low, Q20 is turned off. P3C is set high while P3B is still high to turn on transistor Q22. Thus, the gate of transistor Q13 slowly discharges through resistor R9. By allowing the gate to slowly discharge, the drain current through transistor Q13 slowly decreases thereby reducing the change with respect to time of the drain current. The input signal at pin P3B was positive and returns to ground-return. This turns on transistor Q21 to provide a low impedance clamp to the gate of transistor Q13, thus turning transistor Q13 off. Once pin P3B is set low, P3C can be set low. A low impedance clamp is required to prevent transistor Q13 from falsely turning on due to induced gate voltages caused by rapidly changing positive drain to source voltages that couple through the transfer capacitor. Resistors R7, R8, and R10 are pull down resistors to keep transistors Q20, and Q22 off, and Q21 on for activating the low impedance clamp. The diodes D11 and D12 protect the base to emitter junctions of transistors Q20 and Q21, respectively. Diodes D11 and D12 also prevent the base to emitter junctions of these transistors from entering the zener conduction region when transistor Q20 is off but there is still a +Gate-bias voltage on the gate of transistor Q13, and when transistor Q20 is on but transistor Q21 is off.

Because the bridge is symmetrical, the same operation applies to the transistors Q2 and Q12. Specifically, a positive going pulse with respect to ground-return applied to pin P2A turns on transistor Q12 via the push-pull driver configuration of transistors Q14–Q17 and the transformer T2.

A positive going pulse on pins P4A and P4B turns on transistor Q2 by turning on transistor Q9 and turning off transistor Q10, respectively. Pin P4C is held at ground potential to keep Q2 turned on. A pulse on pin P4B turns on transistor Q10 and thus provides a low impedance clamp to the gate of transistor Q2, turning Q2 off. Diodes D9 and D10 function in the same way as diodes D11 and D12.

In the event that the defibrillation pulse should not be delivered to the heart, pin P5A is set high to direct the pulse to an external load (not shown).

The circuit 10 is used in an implantable defibrillator unit 14 as part of an implantable defibrillation system illustrated in FIG. 2. Typically, the defibrillator unit 14

also includes an arrhythmia detection circuit **16** and a stimulation control circuit **18** connected to both the detection circuit **16** and the output circuit **10**. Defibrillator unit **14**, including the circuits **10**, **16**, and **18**, is of a size whereby it comfortably can be implanted in the abdomen of the patient.

The arrhythmia detection circuit **1** is connected to sensing electrodes **20** implanted in or on the heart. The output circuit **10** is connected to implanted electrodes **22** and **24**, shown mounted on the heart for performing defibrillation. The control circuit **18** is triggered by the arrhythmia detection circuit **16** to trigger the output circuit **10** and apply a defibrillation pulse to the heart across electrodes **22** and **24**. The output circuit **10** is capable of delivering mono-phasic, bi-phasic, tri-phasic, . . . n-phasic, and sequential defibrillation pulses to the heart depending upon the control signals applied to the input signal pins P1A-P5A, P3B, P4B, P3C and P4C. The desired type of defibrillation pulse delivered to the heart is programmed in the control circuit **18** which applies the necessary signals to the appropriate signal pins.

As mentioned previously, transistors Q1 and Q12 determine the multi-phasic nature of the defibrillation pulse, and transistors Q2 and Q13 determine the polarity of the pulse. Transistors Q1 and Q13 are used together to generate positive pulses. Transistors Q2 and Q12 are used together to generate negative pulses. With transistor Q!3 turned on, positive pulses will be generated, the duration of which is determined by the length of time transistor Q1 is turned on. The same is true for negative pulses generated by maintaining transistor Q2 on, and varying the pulse duration by the duration which transistor Q12 is on. To generate multi-phasic pulses, the activation of transistors Q1 and Q13 is followed by the activation of transistors Q2 and Q12, or vice versa, for as many phases of the pulse desired. The actual pulse, whether positive or negative, exponentially decreases in magnitude as it normally would, across capacitor C3.

With reference to FIGS. **1** and **3a-3h**, representative defibrillation pulses which can be delivered to the heart by the output circuit **10** will now be described.

FIG. **3a** illustrates a mono-phasic pulse with positive polarity. To achieve this pulse, input signal pins P3A and P3B are set high and input signal pin P3C is grounded to turn transistor Q13 on. A positive going pulse of a predetermined duration is then obtained by setting pin P1A high to turn on transistor Q1.

FIG. **3b** illustrates a mono-phasic pulse with negative polarity. This is achieved by setting pins P4A and P4B high and setting pin P4C low to turn on transistor Q2. A pulse is then applied to pin P2A to turn on transistor Q12.

FIG. **3c** illustrates a bi-phasic pulse with positive polarity achieved by setting pin P3A and pin P3B high and setting pin P3C low. A pulse is applied to pin P1A, turning transistor Q1 on. Thereafter, pin P4A and pin P4B are set high and pin P4C is set low to turn on transistor Q2. A pulse is then applied to pin P2A to turn on transistor Q12.

FIG. **3d** illustrates a bi-phasic pulse with negative polarity achieved by setting pin P4A and pin P4B high and setting pin P4C low. This turns on transistor Q2. A pulse is then applied to pin P2A, turning on transistor Q12. This creates the negative portion of the bi-phasic pulse. Thereafter, pins P3A and P3B are set high and pin P3C is set low, and a pulse is applied to pin P!A. This turns on transistors Q13 and Q1 to create the positive portion of the bi-phasic pulse.

FIG. **3e** illustrates sequential pulses with positive polarity. This is achieved by setting pin P3A and pin P3B high and setting pin P3C low to turn on transistor Q13. A pulse is then applied to pin P1A, turning transistor Q1 on, and repeated for as many positive pulses needed.

FIG. **3f** illustrates sequential pulses with negative polarity being achieved by setting pins P4A and P4B high and setting pin P4C low to turn on transistor Q2. Repeated pulses are applied to pin P2A to turn on transistor Q12 for as many negative pulses desired. As seen in FIGS. **3e** and **3f**, no voltage is lost across capacitor C3.

FIG. **3g** illustrates a tri-phasic pulse with positive polarity. This is achieved by first setting pin P3A and pin P3B high and setting pin P3C low. A pulse is then applied to pin P1A. Then, pins P4A and P4B are set high and pin P4C set low. A pulse is then applied to pin P2A. Finally, pins P3A and P3B are set high and pin P3C is set low. A pulse is applied to pin P1A.

FIG. **3h** illustrates a tri-phasic pulse with negative polarity. This is achieved by first setting pins P4A and P4B high and setting pin P4C low. A pulse is applied to pin P2A. Then, pins P3A and P3B are set high and pin P3C is set low. A pulse is applied to pin P1A. Finally, pins P4A and P4B are set high and pin P4C is set low. A pulse is then applied to pin P2A.

Energy flow is always from Vcap, through transistor Q1, out through patch+, through the heart, into patch−, through transistor Q13, to ground-return, or from Vcap, through transistor Q12, out through patch−, through the heart, into path+, through transistor Q2, and to ground-return.

The advantages of this output bridge circuit are the independent on/off controls of transistors Q1, Q2, Q12, and Q13. The three control pins P4A, P4B, P4C, and P3A, P3B, and P3C for the gate drive circuits of transistors Q2 and Q13, respectively, allow separate control to turn on and off, and reduce current variations with respect to time. In operation, at least one of the two patch leads path+or patch−is always connected to ground-return. Furthermore, a n-phasic defibrillation pulse can easily be generated by alternating the activation of transistors Q1 and Q13 together, with the activation of transistors Q2 and Q12 together.

The above description is intended by way of example only and is not intended to limit the present invention in any way except as set forth in the following claims.

We claim:

1. An output circuit for use in an implantable defibrillation system, said circuit comprising:

capacitor means for storing a predetermined voltage;

first and second switching means, both connected to said capacitor means and capable of being triggered to active conditions;

a ground-return terminal;

first and second electrode lead terminals connected to said first and second switching means, respectively;

[third and] fourth *and third* switching means connected to said first and second lead terminals, respectively, for selectively connecting said first and second electrode lead terminals, respectively, to said ground-return terminal when triggered to active conditions; and

triggering means for triggering said first and said third switching means to said active conditions to

allow voltage stored by said capacitor means to discharge through said first and second electrode lead terminals in a first polarity, and for triggering said second and fourth switching means to said active conditions to allow voltage stored by said capacitor means to discharge through said first and second electrode lead terminals in a second polarity opposite to said first polarity.

2. The circuit of claim 1, and further comprising first and second push-pull driver circuits; first and second control pins connected to said first and second push-pull driver circuits, respectively; and first and second pulse transformers; said first and second pulse transformers including primary and secondary windings, said secondary windings being connected to said first and second switching means, said primary windings being connected to said push-pull driver circuits, and said first and second switching means being triggered to said active conditions by applying an electrical pulse to said first and second control pins.

3. An implantable defibrillation system for delivering mono-phasic, multi-phasic, and sequential defibrillation pulses to a heart via a pair of electrodes implanted on or about the heart, said system comprising:

an output circuit comprising capacitor means for storing a predetermined voltage, first and second switching means both connected to said capacitor means and capable of being triggered to active conditions;

a ground return terminal;

first and second electrode lead terminals connected, respectively to said first and second switching means and to said pair of electrodes;

[third and] fourth *and third* switching means for selectively connecting said first and second electrode lead terminals, respectively, to said ground return terminal when triggered to active conditions;

a control circuit for selectively triggering said first and said third switching means to said active conditions for allowing voltage stored by said capacitor means to discharge through said first and second electrode lead terminals in a first polarity, and triggering said second and fourth switching means to said active conditions for allowing voltage stored by said capacitor means to discharge through said first and second electrode lead terminals in a second polarity opposite to said first polarity.

4. A method for generating a multi-phasic defibrillation pulse via four independently controlled electrical switching elements for delivery to the heart of a patient via first and second electrodes implanted on or about the heart, said method comprising the steps of:

charging a capacitor to a predetermined voltage;

triggering a first electrical switching element connected to said capacitor and said first electrode to an active condition and triggering a third electrical switching element connected to said second electrode and a ground terminal to an active condition for delivering voltage through said first an second electrodes to the heart in a first polarity;

triggering a second electrical switching element connected to said capacitor and said second electrode to an active condition and triggering a fourth electrical switching element connected to said first electrode and a ground terminal to an active condition for delivering voltage through said first and second electrodes to the heart in a second polarity opposite to said first polarity.

5. An implantable defibrillation system for delivering mono-phasic, multi-phasic and sequential defibrillation pulses to a heart via a pair of discharge electrodes implanted on or about the heart, said system comprising:

sensing electrode means mounted on or about the heart;

arrhythmia sensing means connected to said sensing electrode means for detecting an arrhythmia of the heart;

an output circuit comprising capacitor means for storing a predetermined voltage; first and second switching means connected to said capacitor means and said discharge electrodes, and capable of being triggered to active conditions; a ground return terminal; first and second electrode lead terminals connected, respectively, to said first and second switching means and to said pair of electrodes; [third and] fourth *and third* switching means for selectively connecting said first and second electrode lead terminals, respectively, to said ground return terminal when triggered to active conditions;

control means for selectively triggering said first and said third switching means to said active conditions for allowing voltage stored by said capacitor means to discharge through said first and second electrode lead terminals in a first polarity, and triggering said second and fourth switching means to said active conditions for allowing voltage stored by said capacitor means to discharge through said first and second electrode lead terminals in a second polarity opposite to said first polarity.

* * * * *

MAINTENANCE FEE STATEMENT

The data shown below is from the records of the Patent and Trademark Office. If the maintenance fees and any necessary surcharges have been timely paid for the patents listed below, the notation "PAID" will appear in column 10, "status" below.

If a maintenance fee payment is defective, the reason is indicated by code in column 10, "status" below. An explanation of the codes appears on the reverse of the Maintenance Fee Statement. TIMELY CORRECTION IS REQUIRED IN ORDER TO AVOID EXPIRATION OF THE PATENT. NOTE 37 CFR 1.377. THE PAYMENT(S) WILL BE ENTERED UPON RECEIPT OF ACCEPTABLE CORRECTION. IF PAYMENT OR CORRECTION IS SUBMITTED DURING THE GRACE PERIOD, A SURCHARGE IS ALSO REQUIRED. NOTE 37 CFR 1.20(k) and (l).

If the statement of small entity status is defective the reason is indicated below in column 10 for the related patent number. THE STATEMENT OF SMALL ENTITY STATUS WILL BE ENTERED UPON RECEIPT OF ACCEPTABLE CORRECTION.

ITM NBR	PATENT NUMBER	FEE CDE	FEE AMOUNT	SUR CHARGE	SERIAL NUMBER	PATENT DATE	FILE DATE	PAY YR	SML ENT	STAT
1	4,998,531	183	930	----	07/501,527	03/12/91	03/28/90	04	NO	PAID

If the "status" column for a patent number listed above does not indicate "PAID" a code or an asterisk (*) will appear in the "status" column. Where an asterisk (*) appears, the codes are set out below by the related item number. An explanation of the codes indicated in the "status" column and as set out below by the related item number appears on the reverse of the maintenance fee statement.

ITM NBR	ATTY DKT NUMBER
1	729Y6524

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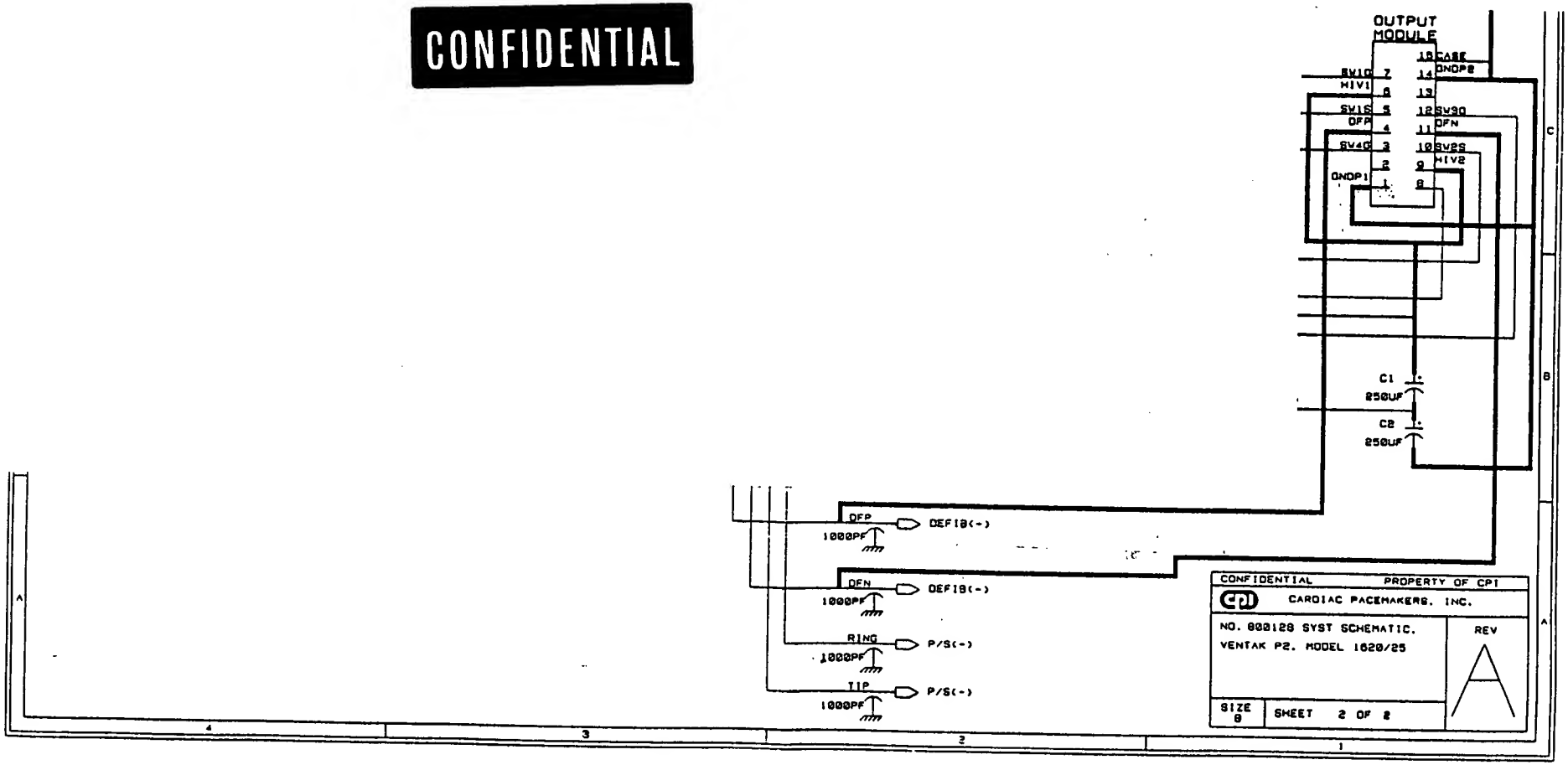

1.0 SCOPE

This document defines the requirements for a high-reliability defibrillation output module hybrid (hereafter called defib output module) to be used in an implantable defibrillator/pacemaker. All precautions relating to the manufacture of this device must be taken to meet the requirements of this document.

2.0 APPLICABLE DOCUMENTS

MIL-STD-883 Test Methods and Procedures for Microelectronics

3.0 FUNCTIONAL DESCRIPTION

3.1 General

The defib output module is divided into identical sides (side A and side B), with each side containing two N-channel IGBT power transistors; four rectifier diodes; and four smaller silicon NPN transistors mounted on a ceramic substrate. The power transistors act as switches to process a high voltage input into the following types of defibrillation output pulses: positive monophasic, negative monophasic, positive biphasic, negative biphasic, positive triphasic, negative triphasic, positive quadraphasic, negative quadraphasic, positive sequential, and negative sequential. The transistors are switched on and off using externally connected gate inputs. The other module components are used for steering purposes and for transient protection.

3.2 Schematic Diagram

The schematic diagram for the defib output module is per Figure 1.

3.3 Device Operation

The defib output module operates identically for side A and side B. This section describes the operation of side A, except where otherwise indicated.

Q401 and Q402 are used as switches. Q401 and Q402 have a 1000 volt breakdown and 100 amp peak current rating. D401 through D404 have a 1000 volt breakdown and 55 amp surge current rating. D401 acts as a body diode to protect the bipolar output structure of Q401. D402 acts

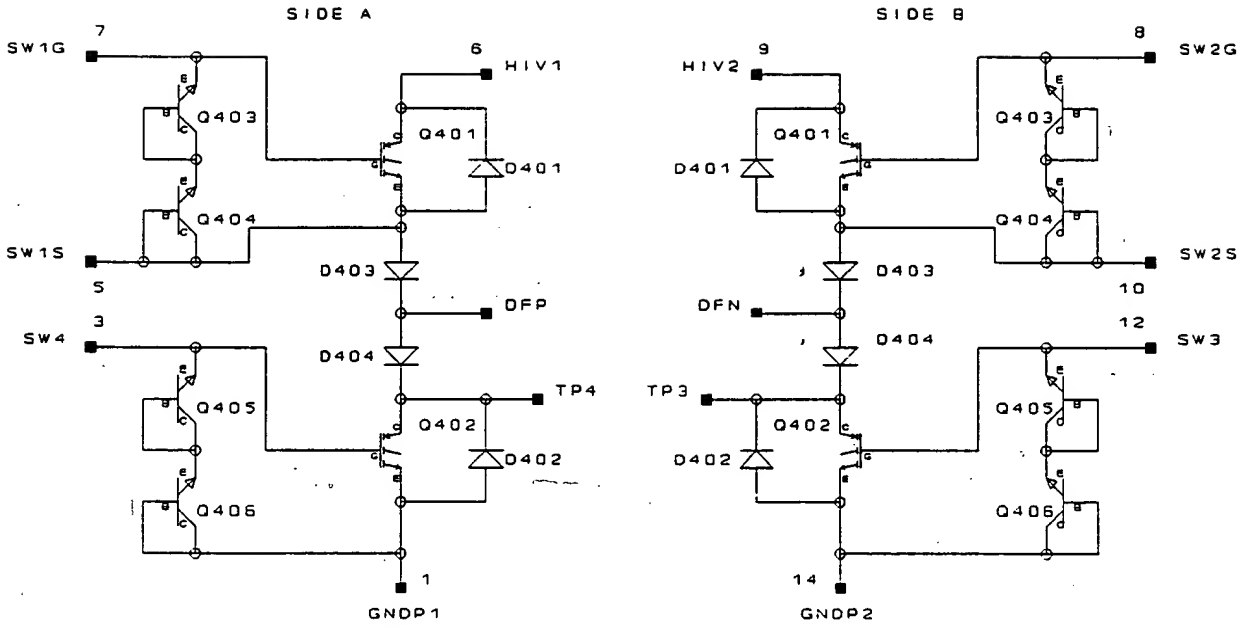

Figure 1. Schematic Diagram

as a body diode to protect the bipolar output structure of Q402. D403 steers the defib output current to the load. D403 also protects Q401 from counter emf potentials developed in the stray lead and load inductances when the opposite side of the bridge delivers a defib output pulse. D403 also protects the defib output bridge when an external voltage is applied between DFP and DFN. D404 steers the defib output current from the load. D404 protects Q402 from counter emf potentials developed in the stray lead and load inductances when the other side of the bridge delivers a defib output pulse. D404 protects the defib output bridge when an external voltage is applied between DFP and DFN.

Q403 through Q406 are small signal transistors configured as diodes. Q403 and Q404 are two series connected diodes. With respect to SW1G to SW1S, the base-emitter breakdown region of the transistors is used as a 12 volt zener to protect the gate-emitter structure of Q401 from induced positive gate-emitter transients. With respect to SW1S to SW1G, the two diodes clip the emitter-gate voltage to within two base-emitter voltage drops to protect the gate-emitter structure of Q401 from induced negative gate-emitter transients. When Q401 is pulsed off under normal operation, these diodes prevent excessive negative gate-emitter voltages from developing. This enhances the turn-on time of the switch. Q405 and Q406 are two series connected diodes. With respect to SW4 to GNDP1, the base-emitter breakdown region of the transistors is used as a 12 volt zener to protect the gate-emitter structure of Q402 from induced positive gate-emitter transients. With respect to SW4 to GNDP1, the two diodes clip the emitter-gate voltage to within two base-emitter voltage drops to protect the gate-emitter structure of Q402 from induced negative gate-emitter transients.

HIV1, HIV2, GNDP1, and GNDP2 are connected externally, and serve as the high voltage supply connections.

For side A, an external transformer-isolated gate driver is connected between SW1G and SW1S. A +12 volt pulse is delivered to the external transformer-isolated gate driver input producing a +12 volt output which is stored in the gate-emitter capacitance of Q401, thereby turning Q401 on. A -12 volt pulse is delivered to the external transformer-isolated gate driver input causing the gate-emitter capacitance to be shorted through a low impedance path, thereby removing the gate-emitter charge and turning Q401 off.

A +12 volt gate bias with respect to GNDP1 is applied at SW4 to turn Q402 on. Turning Q402 off is a three step procedure. First, the +12 volt gate bias is removed. Second, the gate-emitter charge is allowed to exponentially discharge through an external 47 kilohm resistance for 793 microseconds. Third, an external MOSFET switch is turned on to short the gate to the emitter, thereby preventing Q402 from turning on.

For side B, an external transformer-isolated gate driver is connected between SW2G and SW2S. A +12 volt pulse is delivered to the external transformer-isolated gate driver input producing a +12 volt output which is stored in the gate-emitter capacitance of Q401, thereby turning Q401 on. A -12 volt pulse is delivered to the external transformer-isolated gate driver input causing the gate-emitter capacitance to be shorted through a low impedance path, thereby removing the gate-emitter charge and turning Q401 off.

A +12 volt gate bias with respect to GNDP2 is applied at SW3 to turn Q402 on. Turning Q402 off is a three step procedure. First, the +12 volt gate bias is removed. Second, the gate-emitter charge is allowed to exponentially discharge through an external 47 kilohm resistance for 793 microseconds. Third, an external MOSFET switch is turned on to short the gate to the emitter, thereby preventing Q402 from turning on.

The module delivers a positive phased pulse (from DFP to DFN) as follows: Q402, side A, is turned off. Q401, side B, is off. Q402, side B, is turned on. Q401, side A, is turned on. Current flows from the HIV1 pin through Q401 and D403, side A, out the DFP pin into the load. The current returns from the load through the DFN pin, through D404 and Q402, side B, to the GNDP2 pin. Q401, side A, is turned off.

The module delivers a negative phased pulse (from DFN to DFP) as follows: Q402, side B, is turned off. Q401, side A, is off. Q402, side A, is turned on. Q401, side B, is turned on. Current flows from the HIV2 pin through Q401 and D403, side B, out the DFN pin into the load. The current returns from the load through the DFP pin, through D404 and Q402, side A, to the GNDP1 pin. Q401, side B, is turned off.

3.4 Pin Description

The defib output module pins are described in Table 1.

TABLE 1. DEFIB OUTPUT MODULE PIN DESCRIPTION

PIN	LABEL	TYPE	DESCRIPTION
1	GNDP1	Ground	High voltage supply return side A
2	TP4	Input/output	Test point at collector of Q402 side A
3	SW4	Input	Gate of Q402 side A
4	DFP	Output	Defib output side A
5	SW1S	Input	Emitter of Q401 side A
6	HIV1	Supply	High voltage supply side A
7	SW1G	Input	Gate of Q401 side A
8	SW2G	Input	Gate of Q401 side B
9	HIV2	Supply	High voltage supply side B
10	SW2S	Input	Emitter of Q401 side B
11	DFN	Output	Defib output side B
12	SW3	Input	Gate of Q402 side B
13	TP3	Input/output	Test point at collector of Q402 side B
14	GNDP2	Ground	High voltage supply return side B
15	GNDC	Ground	Case ground

4.5 Timing Sequence

Tables 5 through 14 describe the required sequence and timing for the module to deliver the following pulses, respectively: positive monophasic, negative monophasic, positive biphasic, negative biphasic, positive triphasic, negative triphasic, positive quadraphasic, negative quadraphasic, positive sequential, and negative sequential.

TABLE 5. POSITIVE MONOPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 4 is clamped. Switch 3 is unclamped.
2	30.5 μsec	Switch 3 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
6	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 is clamped.

TABLE 6. NEGATIVE MONOPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 3 is clamped. Switch 4 is unclamped.
2	30.5 μsec	Switch 4 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
6	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped.

TABLE 7. POSITIVE BIPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 4 is clamped. Switch 3 is unclamped.
2	30.5 μsec	Switch 3 gate bias is turned on.
3	1.0 to 36.0 msec	Switch 1 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
6	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 is clamped. Switch 4 is unclamped.
7	30.5 μsec	Switch 4 gate bias is turned on.
8	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
9	61.0 μsec	Wait state. No activity.
10	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
11	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped.

TABLE 8. NEGATIVE BIPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 3 is clamped. Switch 4 is unclamped.
2	30.5 μsec	Switch 4 gate bias is turned on.
3	1.0 to 36.0 msec	Switch 2 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.

TABLE 8. NEGATIVE BIPHASIC TIMING SEQUENCE (CONT)

SEQ	TIMING	DESCRIPTION
6	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped. Switch 3 is unclamped.
7	30.5 μsec	Switch 3 gate bias is turned on.
8	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
9	61.0 μsec	Wait state. No activity.
10	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
11	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 is clamped.

TABLE 9. POSITIVE TRIPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 4 is clamped. Switch 3 is unclamped.
2	30.5 μsec	Switch 3 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
6	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 is clamped. Switch 4 is unclamped.
7	30.5 μsec	Switch 4 gate bias is turned on.
8	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
9	61.0 μsec	Wait state. No activity.

TABLE 9. POSITIVE TRIPHASIC TIMING SEQUENCE (CONT)

SEQ	TIMING	DESCRIPTION
10	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
11	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped. Switch 3 is unclamped.
12	30.5 μsec	Switch 3 gate bias is turned on.
13	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
14	61.0 μsec	Wait state. No activity.
15	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
16	30.5 μsec	Switch 3 gate recovery is turned off Switch 3 is clamped.

TABLE 10. NEGATIVE TRIPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 3 is clamped. Switch 4 is unclamped.
2	30.5 μsec	Switch 4 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
6	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped. Switch 3 is unclamped.
7	30.5 μsec	Switch 3 gate bias is turned on.

TABLE 10. NEGATIVE TRIPHASIC TIMING SEQUENCE (CONT)

SEQ	TIMING	DESCRIPTION
8	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
9	61.0 μsec	Wait state. No activity.
10	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
11	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 is clamped. Switch 4 is unclamped.
12	30.5 μsec	Switch 4 gate bias is turned on.
13	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
14	61.0 μsec	Wait state. No activity.
15	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
16	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped.

TABLE 11. POSITIVE QUADRAPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 4 is clamped. Switch 3 is unclamped.
2	30.5 μsec	Switch 3 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.

TABLE 11. POSITIVE QUADRAPHASIC TIMING SEQUENCE (CONT)

SEQ	TIMING	DESCRIPTION
6	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 is clamped. Switch 4 is unclamped.
7	30.5 μsec	Switch 4 gate bias is turned on.
8	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
9	61.0 μsec	Wait state. No activity.
10	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
11	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped. Switch 3 is unclamped.
12	30.5 μsec	Switch 3 gate bias is turned on.
13	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
14	61.0 μsec	Wait state. No activity.
15	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
16	30.5 μsec	Switch 3 gate recovery is turned off Switch 3 is clamped. Switch 4 is unclamped.
17	30.5 μsec	Switch 4 gate bias is turned on.
18	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
19	61.0 μsec	Wait state. No activity.
20	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
21	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped.

TABLE 12. NEGATIVE QUADRAPHASIC TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 3 is clamped. Switch 4 is unclamped.
2	30.5 μsec	Switch 4 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
6	30.5 μsec	Switch 4 gate recovery is turned off Switch 4 is clamped. Switch 3 is unclamped.
7	30.5 μsec	Switch 3 gate bias is turned on.
8	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
9	61.0 μsec	Wait state. No activity.
10	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
11	30.5 μsec	Switch 3 gate recovery is turned off Switch 3 is clamped. Switch 4 is unclamped.
12	30.5 μsec	Switch 4 gate bias is turned on.
13	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
14	61.0 μsec	Wait state. No activity.
15	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
16	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 is clamped. Switch 3 is unclamped.

TABLE 12. NEGATIVE QUADRAPHASIC TIMING SEQUENCE (CONT)

SEQ	TIMING	DESCRIPTION
17	30.5 μsec	Switch 3 gate bias is turned on.
18	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
19	61.0 μsec	Wait state. No activity.
20	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
21	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 is clamped.

TABLE 13. POSITIVE SEQUENTIAL TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 4 is clamped. Switch 3 is unclamped.
2	30.5 μsec	Switch 3 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 1 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 3 gate recovery is turned on. Switch 3 gate bias is turned off.
6	30.5 μsec	Switch 3 gate recovery is turned off. Switch 3 gate bias is turned on. Sequence steps 2 through 6 may be repeated up to three times. For the third time, instead of turning switch 3 gate bias on, switch 3 is clamped.

TABLE 14. NEGATIVE SEQUENTIAL TIMING SEQUENCE

SEQ	TIMING	DESCRIPTION
1	30.5 μsec	Switch 3 is clamped. Switch 4 is unclamped.
2	30.5 μsec	Switch 4 gate bias is turned on.
3	1.0 msec to 36.0 msec	Switch 2 is turned on and off to fire pulse.
4	61.0 μsec	Wait state. No activity.
5	793.0 μsec	Switch 4 gate recovery is turned on. Switch 4 gate bias is turned off.
6	30.5 μsec	Switch 4 gate recovery is turned off. Switch 4 gate bias is turned on. Sequence steps 2 through 6 can be repeated up to three times. Upon the last time, instead of turning switch 4 gate bias on, switch 4 is clamped.